Advance Information

This document contains information on a product under development. The parametric and functional information are target parameters and are subject to change without notice. Please consult Brooktree regarding the most updated datasheet before design.

Bt463

170 MHz Monolithic CMOS TrueVu™ RAMDAC™

Distinguishing Features

- 170, 135, 110 MHz Operation
- Multiple Display Modes on a Pixel Basis
- Multiple Color Maps
- Variable Palette Sizes
- Up to 8 Overlay Planes
- Reconfigurable Pixel Port
- 1:1, 2:1 or 4:1 Multiplexed Pixel Ports
- Three 528 x 8 Color Palette RAMs
- Programmable Setup (0 or 7.5 IRE)
- X Windows Support
- Input and Output Signature Registers
- JTAG Support
- 169-pin PGA Package

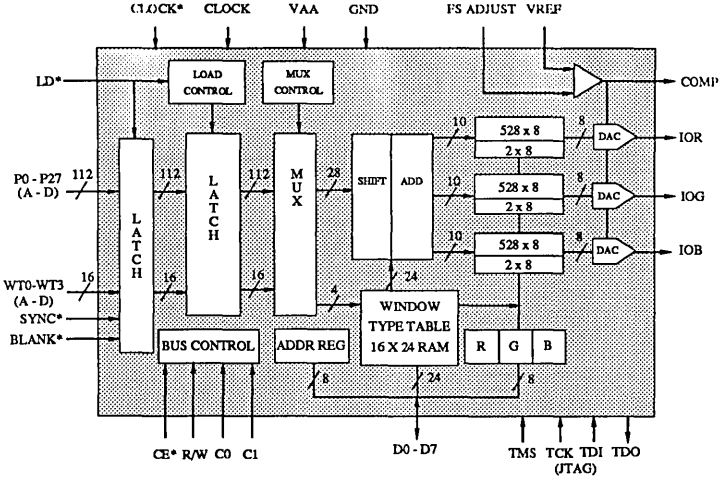
Applications

- High Resolution Color Graphics
- Medical Imaging
- Visualization
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt438

Functional Block Diagram



Product Description

The Bt463 is a high performance RAMDAC designed specifically for true color and pseudo color graphics addressing multiple lookup tables for different windows. It has three 528 x 8 look-up tables with triple 8-bit D/A converters to support 24-bit true color and 9-bit pseudo color operation.

The TrueVu™ RAMDAC allows different display modes of operation for each pixel. Utilizing a proprietary window type scheme, each set of pixel and overlay data has four type bits which map the accompanying pixel data to a user-defined display mode. The type bits address a window type table which ultimately determines the description of the pixel data. With this scheme, arbitrary plane depth and unique visual display type can be achieved on a pixel basis. For example, separate windows displaying 24-plane true color, 8-plane pseudo color, and 12-plane double-buffer true color, each with a separate color map, can exist within a single frame. The size of each individual lookup table is user-configurable and can vary from 16 to 512 addresses.

On-chip features include programmable 1:1, 2:1, or 4:1 input multiplexing of the pixels, bit plane masking, and a programmable setup (0 or 7.5 IRE). The Bt463 has significant testability features, including input and output signature analysis registers, and fully supports the JTAG specification.

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Architecture

Introduction

With X Windows becoming the de facto standard, the need for each window to have its unique color map and display type becomes apparent. Each window should be able to use its own private color map and define its own interpretation of pixel values in the frame buffer using a variety of possible visual types. In addition, since each window is completely independent of other windows, the hardware must be able to accommodate multiple visual types within a single frame of graphics display. Thus, the ability to switch to different color maps and visual types on a pixel-by-pixel basis is essential. The Bt463 has been designed specifically to address multiple windows and display types. The Bt463 is extremely flexible, permitting multiple visual types to be displayed simultaneously and efficiently supporting multiple virtual color maps within the physical color map.

Overview

Window type data is sent to the TrueVu™ RAMDAC along with each pixel. The window type addresses a 16 x 24 window type table, which converts pixels from a virtual color map index to a physical color map index prior to sending them to the lookup table. In addition to specifying the physical color map location and display type, the window type table can determine the number of planes, location of the frame buffer data, location of overlay data, and select specific overlay planes for each window.

Even though the Bt463 has 24-plane true color capability, the assignment of red, green, and blue pins is not fixed to preassigned locations. The Bt463 is flexible, allowing pixel or overlay data to be in practically any location of the 28-bit pixel/overlay word and be shifted into position to address the lookup table. With this flexibility, the Bt463 can be configured in a variety of ways. A number of possible configurations are listed in Table 1.

Pixel Pin Location	Mapped Function	Display Mode
P0–P7 P8–P15 P16–P23 P24–P27	R0-R7 G0-G7 B0-B7 OL0-OL3	24-bit true color 4-plane overlay
P0–P8 P24–P27	P0-P8 OL0-OL3	9-bit pseudo color 4-plane overlay
P8–P15 P16–P19	P0–P7 OL0–OL3	8-bit pseudo color 4-plane overlay
P0–P7 P8–P15 P16–P23 P24–P27, WT0–WT3	R0–R7 G0–G7 B0–B7 OL0–OL7	24-bit true color 8-plane overlay
P4–P7 P12–P15 P20–P23 P24–P27	R0–R3 G0–G3 B0–B3 OL0–OL3	12-bit true color 4-plane overlay
P1–P7 P9–P15 P18–P23 P16, P8, P0, P17	R1–R7 G1–G7 B2–B7 OL0, OL1, OL2, OL3	24-bit true color 4-plane overlay

Table 1. Example Pixel/Overlay Configurations and Display Modes.

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt463 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers, window type table, and color palettes. The dual-port color palette RAMs allow color updating without contention with the display refresh process.

As illustrated in Table 2, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 12-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit. ADDR0 and ADDR8 correspond to data bus bit D0. ADDR12–ADDR15 are ignored during MPU write cycles and return a logical zero when read by the MPU.

The control registers and window type table are also accessed through the address register in conjunction with the C0 and C1 inputs, as shown in Table 2. All control registers may be written to or read by the MPU at any time. When accessing the control registers, window type table and the color palette RAM, the address register increments following a read or write cycle.

Writing/Reading Color Palette RAM

To write color data, the MPU loads the address register with the address of the color palette RAM or cursor color register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select the color palette RAM or cursor color register. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read the color palette RAM or cursor color register, the MPU loads the address register with the address of the color palette RAM location or cursor color register to be read. Reading color data is similar to writing, except the MPU executes read cycles.

When accessing the cursor color registers, the address register increments to $0102 following a blue read or write cycle. The color palette RAM does not have a wraparound feature after the last valid address. However, any attempt to write past $020F does not affect previous data load cycles. The address register will reset to $0000 after incrementing past $0FFF.

Writing/Reading Window Type Table

To write the window type table, the MPU writes the address register with the table location to be modified. The MPU performs three successive write cycles (B0–B7, B8–B15, then B16–B23) with B0 being the least significant bit, using C0 and C1 to select the window type table. B0, B8, and B16 correspond to data bus bit D0. After the third write cycle, the three bytes of the table entry are concatenated into a 24-bit word and written to the window type table address specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of three bytes to the window type table. To avoid irregular window displays on the screen, MPU accesses to the window type table are restricted to horizontal and vertical retrace periods.

ADDR0 - 16	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0–7)
$xxxx	01	address register (ADDR8–11)
$0100	10	cursor color 0*
$0101	10	cursor color 1*
$0200	10	ID register ($2A)
$0201	10	command register_0
$0202	10	command register_1
$0203	10	command register_2
$0205	10	P0–P7 read mask register
$0206	10	P8–P15 read mask register
$0207	10	P16–P23 read mask register
$0208	10	P24–P27 read mask register
$0209	10	P0–P7 blink mask register
$020A	10	P8–P15 blink mask register
$020B	10	P16–P23 blink mask register
$020C	10	P24–P27 blink mask register
$020D	10	test register
$020E	10	input signature register**
$020F	10	output signature register*
$0220	10	revision register ($A)
$0300–$030F	10	window type table*
$0000–$020F	11	color palette RAM*

*Indicates requires three read/write cycles
** Indicates 2 out of 3 valid read/write cycles

Table 2. Address Register (ADDR) Operation.

Circuit Description (continued)

To read the window type table data, the MPU loads the address register with the address of the type table to be read. Contents of the type table are copied into a 24-bit register and the address register is incremented to the next window type table entry. The MPU performs three successive read cycles (B0–B7, B8–B15, then B16–B23) with B0 being the least significant bit, using C0 and C1 to select the window type table. B0, B8, and B16 correspond to data bus bit D0.

Additional Information

When accessing the color palette RAM, window type table, signature analysis registers, or cursor color registers, the address register increments after every third read/write cycle for each addressable location. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0–11) are accessible to the MPU.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

For 8-bit registers, the address increments after every read/write cycle.

Figure 1 illustrates the MPU read/write timing of the Bt463.

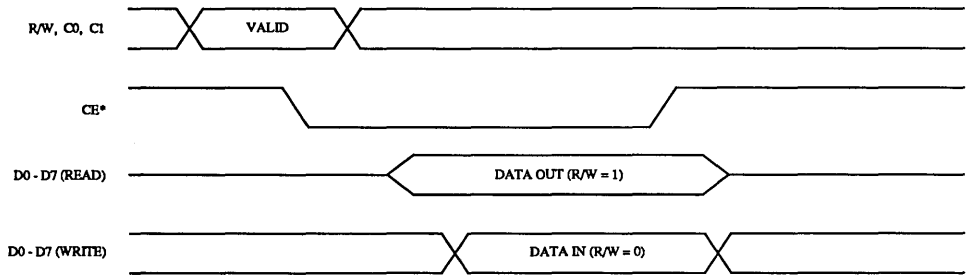


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt463 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, window type, and overlay information, for either one, two, or four consecutive pixels, are latched into the device. Note that with this configuration, the sync and blank timing will be recognized only with one, two, or four pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs.

For 1:1, 2:1, or 4:1 input multiplexing, the Bt463 outputs color information each clock cycle based on the (A) inputs, followed by the (B) inputs, etc., until one, two, or four pixels have been output, at which point the cycle repeats.

To simplify the frame buffer interface timing, LD* may be phase-shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by two or four, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than three, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 1:1 multiplexing is specified, the CLOCK and CLOCK* signals are ignored and pixel data is latched on the rising edge of LD*. If 2:1 multiplexing is specified, only one rising edge of LD* should occur every two clock cycles. If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

Color Palette RAM

The color lookup table consists of three independent RAMs with variable size color maps. Multiple color maps can be assigned within each of the three 528 x 8 lookup tables with the minimum color map size being 16 colors. The color map can be as large as 512 colors.

Color generated by pixel or overlay data is independent of the absolute physical address of the lookup table. Pixel, overlay, and underlay data is referenced relative to its own color map. The start address indicating the beginning of each physical color map is added to the

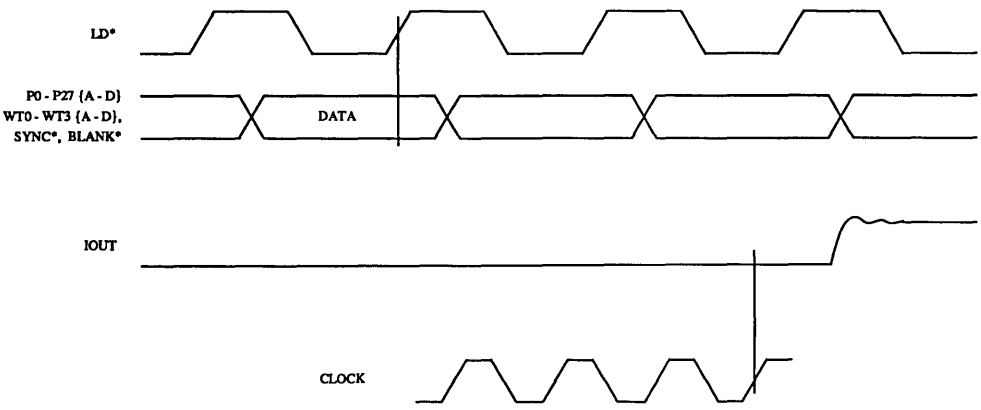


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

pixel data to generate the address for the final color. The start address is specified through the window type table.

Window Type Table

Window type data is sent to the RAMDAC along with each pixel. The window type addresses a 16 x 24 window type table selecting one of sixteen 24-bit window type words. The window type word reconfigures the mapping of the input pixels to the RAMDAC, pixel by pixel. Each color map requires a pointing index to convert pixels from a virtual color map index to a physical color map index. In addition to specifying the physical color map location and display type, the window type table can determine the number of planes, location of the frame buffer data, and location of overlay data, and can select specific overlay planes for each window.

Even though the Bt463 has 24-plane true color capability, the assignment of red, green, and blue pins is not fixed to preassigned locations. The Bt463 is flexible, providing capabilities to have pixel or overlay data in practically any location of the 28-bit pixel/overlay word. The pixels are shifted into position where they address the lookup table. With this flexibility, the Bt463 can be configured in a variety of ways, such as those listed in Table 1.

Associated with each set of pixel data is a 4-bit window type word (WT0–WT3). The window type addresses one of 16 possible entries of the window type table. Each 24-bit window type entry is associated with a particular configuration mode which specifies the number of planes, window display type, start address of the physical color map, shift constant, overlay location, and bypass operation. Multiple windows utilizing the same configuration mode can address the same entry of the window type table, as illustrated in Figure 3. It is recommended that the window type table be loaded by the MPU during vertical retrace to minimize disruptions during the display process.

The window type table provides the capability to switch back and forth between different display modes and individual color maps on a pixel-by-pixel basis. For example, the Bt463 can switch from 24-plane true color to 12-plane true color to 8-plane pseudo color, all within a single frame of graphic data. This allows users to personalize color maps specific to individual windows.

Users have the option of designating the 15th and 16th codes of the window type table to be used as a cursor. These two window type codes directly address the cursor palette, bypassing all pixel manipulation operations. This feature eliminates the need to use the overlay ports as an interface to a hardware cursor. Window type $E is defined as cursor color 0 and $F is cursor color 1.

The window type table words consist of 7 different fields which map the function of the accompanying pixel data. The 7 fields, shown in Figure 4 are: shift, number of planes, display mode, overlay location, overlay mask, start address and lookup table bypass. These fields are described in detail in the following sections.

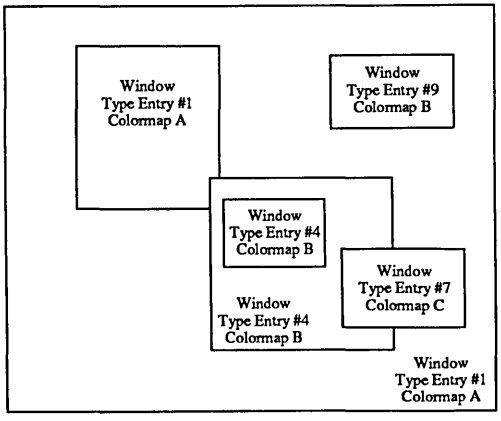


Figure 3. Multiple Windows Utilizing Different Color Maps.

Circuit Description (continued)

Window Type Table Fields

Shift <B4:B0>

This field specifies the plane position where active planes begin. If the active planes are in higher order bits, the shift field can shift these bits into the least significant position which will address the RAM. For instance, a value of 8 specifies active planes to begin at position P8. This field is particularly useful for double buffer applications. The shift value applies to the entire 28-bit pixel/overlay input. Legal values are 0 through 27. However, the number of planes plus the shift value should not exceed 28 within one window type table entry.

Number of Planes <B8:B5>

This field determines the number of active planes used for pixel data. Zeros will be inserted in bit planes above the specified MSB. For true color modes, the appropriate value in this field corresponds to the number of planes per channel. For instance, a 24-plane true color window should specify 8 as the number of planes. Legal values for this field are 0 through 8 for true color and 0 through 9 for pseudo color windows. Zero planes correspond to the color at the start address location regardless of pixel data, dependent on overlay and cursor data. This is useful for generating background color or flood color while the window is being changed or moved. The number of planes plus the shift value should not exceed 28 for the pseudo color mode. The number of planes times 3 plus the shift value shound not exceed 28 for the true color mode.

Display Mode <B11:B9>

This field determines the display mode of the pixel data. Valid display options are true color, pseudo color, bank select, 12-plane double buffer true color and pseudo color with load interleave. Refer to Table 3 for full display mode descriptions.

Overlay Location <B12>

The overlay location field specifies the source location of the overlay planes. A logic zero specifies overlay data to come from P<27:24>. The overlay location is fixed to these four pixel locations, unaffected by any shift in the shift fields. A logic one in this field specifies overlay data to come from the least significant bits of the pixel data (true color mode) or the four planes above the pixel planes (pseudo color mode). The overlay locations for the true color mode are P<17, 0, 8, 16>, with P16 being the LSB of the overlay word. The overlay location is affected by the shift value and only utilizes these variable locations after the shift operation has been completed.

Overlay Mask <B16:B13>

The overlay mask field is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette. B13 corresponds to OL0. B13–B16 are logically ANDed with the corresponding overlay plane input. The selected overlay planes are then compacted into the LSB positions with the higher significant bits filled with zeroes. This feature allows the user to assign specific overlay planes to individual windows. Two or more separate overlay images can be generated independently and switched on a pixel-by-pixel basis using the same or different overlay palette.

Start Address <B22:B17>

The start address specifies the beginning of the physical address of each individual color map. Pixel data addresses the lookup table independently of the absolute physical location of the color map. The start address constitutes the 6 MSBs of the start rows of the color maps. Color address is generated by adding the pixel data with the start address in the physical color map. The maximum valid physical address resulting from this addition is $020F. Color maps start on 16 row boundaries and are allocated in blocks of 16. Thus a binary value of 000001 corresponds to the physical address location of $0010. It is not necessary to fill the entire block with color map colors. The resultant value from pixel data plus the start address should not exceed the 528 address space of the lookup table. Various color maps can be disjoint, overlapping or subsets of other color maps. Minimum color map size is 16 while the maximum contiguous color map size is 512 colors. Legal values are 000000 through 100000.

Lookup Table Bypass <B23>

Up to 24 bits of pixel information are input via P0–P27 inputs. Even in the bypass mode, pixel manipulation still occurs with the 8 lowest significant bits used for each DAC. After shifting, pixels which are positioned in the LSB positions, P0–P7, are mapped as R0–R7, bypass the red color palette, and drive the red DAC directly. Similarly, P8–P15 pixels are mapped as G0–G7 and drive the green DAC directly. P16–P23 are mapped as B0–B7 and drive the blue DAC directly. The bypass mode can only be used in the 8-plane mode.

With the display mode set to pseudo color, the bypass bit will generate 256 shades of gray scale. Eight bits of color information are applied equally to each of the three DACs.

In the bypass mode, overlays are still effective in either the 4- or 8-plane mode and address the overlay palette.

Circuit Description (continued)

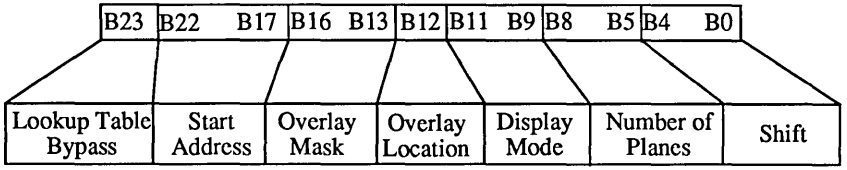


Figure 4. Window Type Table Fields.

Display Mode	Field	Description
True Color	000	An equal number of red, green, and blue pixel planes are input via the pixel port. The number of bits of true color is dependent on the "number of planes" field in the window type table. Eventually, pixel data must be shifted so that the least significant bit of the red pixel word is P0, green is P8, and blue is P16. Number of planes per channel is 0 to 8 for this mode. Correspondingly, the number of planes for the pixel data is three times the value in this field for true color. For example, a value of 8 in the plane field yields 24-plane true color. A value of 4 in the plane field yields a 12-plane true-color configuration.
Pseudo Color	001	All three color palette RAMs are addressed by the same planes of pixel data. Pixel data for the pseudo color must come from a contiguous set of planes. Maximum number of active planes is nine for the pseudo color mode. Number of available planes range from 0 to 9.
Bank Select	010	Overlay bits are concatenated as the MSBs to the pixel data to address a different portion of the lookup table without changing pixel data. Bank select is especially useful for highlighting or color contrasting by changing overlay inputs instead of regenerating the frame buffer image. Number of planes per channel is 0 to 8. Planes used for bank select are also dependent on the overlay mask. Refer to Figure 5 for more details on the bank select mode.
	011	Reserved
Twelve Plane True Color (Load Interleave) See Figure 6.	100	Twelve plane true color is generated by utilizing the lower or upper nibble (4 bits) from 8 bits each of red, green, and blue. Either the upper or lower nibbles are latched on each load clock across a scan line depending on the value of the shift field immediately after blank has been substantiated. The load cycle will begin with the lower nibble for a shift value of $00. If the shift value is $04 immediately after blank, the load cycle will begin with the upper nibble. The output sequence continues to alternate between lower nibble and upper nibble for each load sequence throughout the entire scan line. This display mode preassigns the mapped function for the pixel inputs. P0–P7 is red, P8–P15 is green, and P16–P23 is blue. Refer to Table 4 for more details.
Pseudo Color (Load Interleave) See Figure 6.	101	Eight plane pseudo color data is generated from either the lower nibble bits or upper nibble bits of red and green pixel data. The green nibble bits are concatenated with the red nibble bits to generate the 8 bit pseudo color pixel word. The red nibble comprise the least significant bits. Either the upper or lower nibbles are latched on each load clock across a scan line depending on the value of the shift field immediately after blank has been substantiated. The load cycle will begin with the lower nibble for a shift value of $00. If the shift value is $04 immediately after blank, the load cycle will begin with the upper nibble. The output sequence continues to alternate between lower nibble and upper nibble for each load sequence throughout the entire scan line. Refer to Table 5 for more details.
	110	Reserved
	111	Reserved

Table 3. Display Mode Options.

Circuit Description (continued)

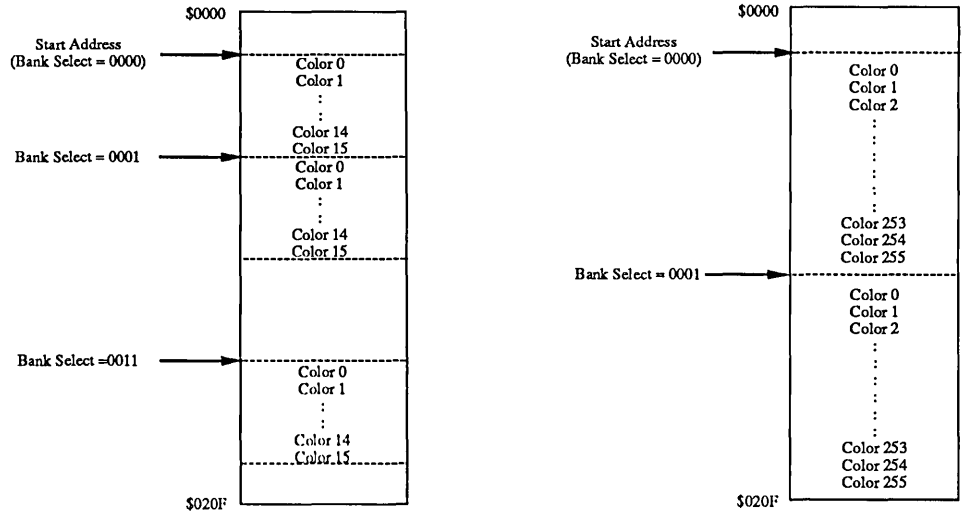


Figure 5. Color Map Allocation using Bank Select.

Pixel Location	Mapped Function	Pixel Word 12-bit True Color Lower Nibble	Lower Nibble Output Sequence	Pixel Word 12-bit True Color Upper Nibble	Upper Nibble Output Sequence
P0–P7 P8–P15 P16–P23	R0–R7 G0–G7 B0–B7	R0–R3 G0–G3 B0–B3	$A_LB_LC_LD_L$	R4–R7 G4–G7 B4–B7	$A_HB_HC_HD_H$

Table 4. 12-Bit True Color (Load Interleave) Mapping and Output Sequence.

Pixel Location	Mapped Function	Pixel Word 8-bit Pseudo Color Lower Nibble	Lower Nibble Output Sequence	Pixel Word 8-bit Pseudo Color Upper Nibble	Upper Nibble Output Sequence
P0–P7 P8–P15 P16–P23	R0–R7 G0–G7 B0–B7	G0–G3, R0–R3	$A_LB_LC_LD_L$	G4–G7, R4–R7	$A_HB_HC_HD_H$

Table 5. 8-Bit Pseudo Color (Load Interleave) Mapping and Output Sequence.

Circuit Description (continued)

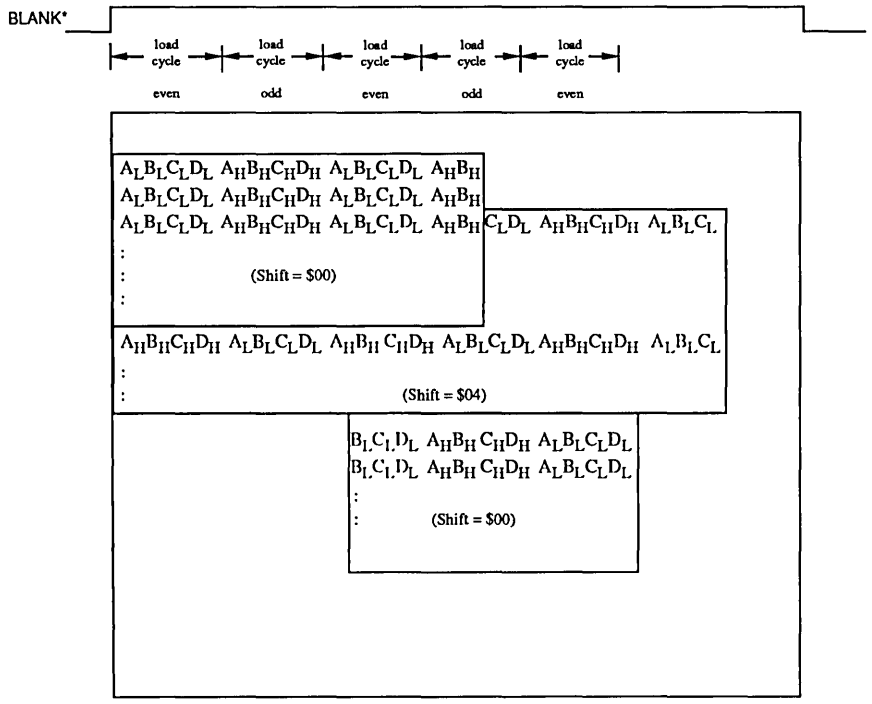


Figure 6. Load Interleave Output Sequence.

Video Generation

Every clock cycle, the color information (up to 24 bits) is presented to the three 8-bit D/A converters.

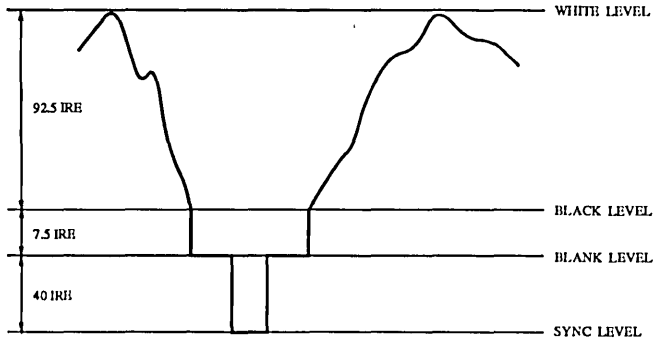
The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 7 and 8. Command Register_2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated, and whether or not sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 6 and 7 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt463 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full scale output current against temperature and power supply variations.

Circuit Description (continued)

SYNC DISABLED		SYNC ENABLED	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly terminated load, RSET = 523 Ω, VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 7. Composite Video Output Waveform (SETUP = 7.5 IRE).

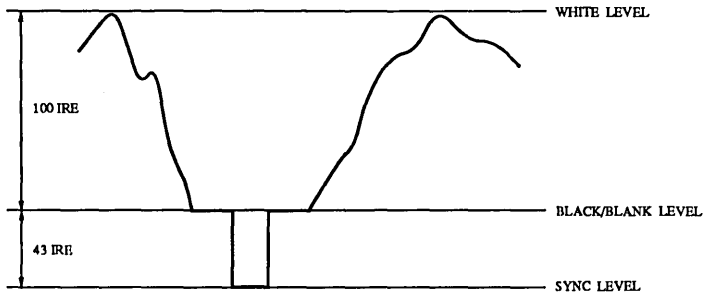
Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 523 Ω, VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 6. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

SYNC DISABLED		SYNC ENABLED	
MA	V	MA	V
18.60	0.698	26.67	1.000
0.00	0.000	8.05	0.302
		0.00	0.000



Note: 75 Ω doubly terminated load, RSET = 495 Ω, VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 8. Composite Video Output Waveform (SETUP = 0 IRE).

Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 495 Ω, VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 7. Video Output Truth Table (SETUP = 0 IRE).

Circuit Description (continued)

Overlay and Underlay Operation

The Bt463 has capabilities for multiple plane overlay and underlay operation. Instead of a dedicated overlay color palette, the overlay palette may be indexed to each of the independent color maps as specified by the user. Overlay color is determined by subtracting $10 from the start address referenced in the window type table and adding the overlay value.

Overlay data can originate from a number of sources. The source location of the overlays is determined by the window type word and command register. All display modes have the capability of utilizing pixel ports 24 to 27 for the overlay address. In addition, for pseudo color applications, the overlay information can originate from the four planes above the pixel planes. For instance, if pixel information is being addressed from P0 to P7, then overlay planes may come from P8 through P11, with P8 being the LSB of the overlay word.

For true color applications, overlay information can also be addressed from the least significant bits of the red, green, and blue pixel data. Two LSBs are used from the blue pixel port. The overlay word <OL3:OL0> consists of P17, P0, P8, and P16 (after shift operation), with P16 being the LSB of the overlay word. The overlay enable mask bits designate whether some or all of the LSB pixel data is to be used as overlay planes.

Instead of multiple overlay palettes, the user can choose a fixed overlay location for all window type entries. The location of the common overlay palette is fixed, independent of the start address of the window type table. The common overlay palette is located at addresses $0201 to $020F.

Underlay operations with various planes can be achieved by changing command register bit CR12 to underlay operation. Once this bit is set for underlay operation, OL3 determines whether the remaining overlay planes should be interpreted as overlay or underlay. If underlays are unavailable as specified in the command register, then the overlay ports are restricted to cursor and overlay operation only. To obtain overlay and underlay operation, the overlay mask must be set to $F. All other values of the overlay mask would result in a compacted overlay word, yielding only underlay operation.

In the standard mode, the Bt463 utilizes 4 overlay/underlay planes providing a palette of 16 colors. However, the Bt463 has a special mode where the window type bits serve as the upper nibble to the overlay port. By setting a command register bit, 8 overlay planes become available. However, no window operation is available as these window type ports are used strictly for overlay ports. Hardware cursor is still available through OL0 and OL1. Both true color and pseudo color operation are available in the 8 overlay plane mode. The physical location of the overlay palette is fixed to a preassigned location.

If a color map start address is specified to be $0000, then overlay colors are located at physical address $0201 to $020F. For other start addresses, refer to Figure 9 for a diagram showing the overlay and pixel palette color map scheme. Tables 8 and 9 provide details of overlay operation for different modes of operation.

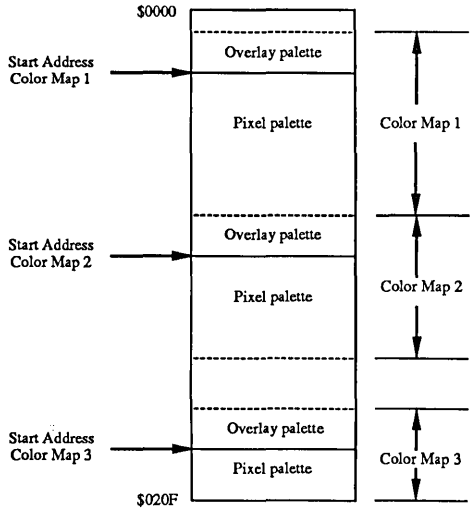


Figure 9. Overlay and Pixel Palette Color Map Scheme.

Circuit Description (continued)

Display Mode	Window Type Field <B11:B9>	Overlay Location <B12>	Overlay Location <OL3:OL0>
True Color	000 000	0 1	P <27:24> P <17, 0, 8, 16>
Pseudo Color	001 001	0 1	P <27:24> P <planes+3:planes>
Bank Select	010 010	0 1	P <27:24> P <17, 0, 8, 16>
12 Plane True Color (Load Interleave)	100 100	0 1	P <27:24> P <17, 0, 8, 16>
Pseudo Color (Load Interleave)	101 101	0 1	P <27:24> not available

Table 8. Overlay Location Truth Table.

Underlay Enable (CR12)	Mapped Function <OL3 : OL0>	Pixel Port <P9:P0>	Physical Ram location Addressed by frame buffer	Operating Mode
x x : x	0000 0000 : 0000	$000 $001 : $1FF	Start Address + $000 Start Address + $001 : Start Address + $1FF	pixel data
0 : 0 0	1111 : 0010 0001	$xxx : $xxx $xxx	Start Address–$10+ $F : Start Address–$10 + $2 Start Address–$10 + $1	overlay only
1 1 1 1 1 1 1 1	1111 1110 1101 1100 1011 1010 1001 1000	$xxx $xxx $xxx $xxx $xxx $xxx $xxx $xxx	Start Address–$10 + $F Start Address–$10 + $E Start Address–$10 + $D Start Address–$10 + $C Start Address–$10 + $B Start Address–$10 + $A Start Address–$10 + $9 Start Address–$10 + $8	overlay
1 1 1 1 1 1 1	0111 0110 0101 0100 0011 0010 0001	$000 $000 $000 $000 $000 $000 $000	Start Address– $10 + $7 Start Address–$10 + $6 Start Address–$10 + $5 Start Address–$10 + $4 Start Address–$10 + $3 Start Address–$10 + $2 Start Address–$10 + $1	underlay

Table 9. Palette and Overlay Select Truth Table (No Hardware Cursor Interfacing the Overlay Port) CR<11:10> = 00, B<16:13> = $F.

Circuit Description (continued)

Hardware Cursor Interface

The Bt463 has numerous configurations for interfacing with a hardware cursor. Utilizing two entry codes of the window type table for a two-color cursor provides the best method of maximizing overlay plane availability without sacrificing a large number of window type entries.

Otherwise, the overlay ports can be used directly as cursor ports but require setting command register bits CR10 and CR11 to configure the RAMDAC for either a single plane cursor or dual-plane cursor through the overlay port. Adding cursor planes through the overlay port reduces the available colors for overlays and underlays.

One Plane Cursor (Overlay Port)

In the one-cursor plane mode, OL0 directly addresses the cursor color palette and overrides all other inputs. By setting a command register, mapped function OL3 determines whether OL1 and OL2 serve as overlay or underlays. Only seven combinations of overlays/ underlays are available. Refer to Table 10 for more details.

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Underlay Enable (CR12)	Mapped Function <OL3 : OL0>	Pixel Port <P9:P0>	Physical Ram Location Addressed by Frame Buffer	Operating Mode
x	0000	$000	Start Address + $000	
x	0000	$001	Start Address + $001	pixel
:	:	:	:	data
x	0000	$1FF	Start Address + $1FF	
x	xxx1	$xxx	Cursor Color 0	cursor
0	1110	$xxx	Start Address–$10 + $E	
0	1100	$xxx	Start Address–$10 + $C	
0	1010	$xxx	Start Address–$10 + $A	overlay
0	1000	$xxx	Start Address–$10 + $8	only
0	0110	$xxx	Start Address–$10 + $6	
0	0100	$xxx	Start Address–$10 + $4	
0	0010	$xxx	Start Address–$10 + $2	
x	xxx1	$xxx	Cursor Color 0	cursor
1	1110	$xxx	Start Address–$10 + $E	
1	1100	$xxx	Start Address–$10 + $C	overlay
1	1010	$xxx	Start Address–$10 + $A	
1	1000	$xxx	Start Address–$10 + $8	
1	0110	$000	Start Address–$10 + $6	
1	0100	$000	Start Address–$10 + $4	underlay
1	0010	$000	Start Address–$10 + $2	

Table 10. Palette and Overlay Select Truth Table (One Plane Hardware Cursor Interfacing the Overlay Port) CR<11:10> = 01, B<16:13> = $F.

Circuit Description (continued)

Two Plane Cursor (Overlay Port)

In the two-cursor plane mode, both mapped functions OL0 and OL1 become cursor planes with OL0 being the least significant bit. With the underlay enabled, OL3 determines whether OL2 serves as an overlay or an underlay. Refer to Table 11 for more details.

Underlay Enable (CR12)	Mapped Function <OL3 : OL0>	Pixel Port <P9:P0>	Physical Ram location Addressed by frame buffer	Operating Mode
x	0000	$000	Start Address + $000	
x	0000	$001	Start Address + $001	pixel
:	:	:	:	data
x	0000	$1FF	Start Address + $1FF	
x	xx01	$xxx	Cursor Color 0	cursor
x	xx1x	$xxx	Cursor Color 1	
0	1100	$xxx	Start Address–$10 + $C	overlay
0	1000	$xxx	Start Address–$10 + $8	only
0	0100	$xxx	Start Address–$10 + $4	
x	xx01	$xxx	Cursor Color 0	cursor
x	xx1x	$xxx	Cursor Color 1	
1	1100	$xxx	Start Address–$10 + $C	overlay
1	1000	$xxx	Start Address–$10 + $8	
1	0100	$000	Start Address–$10 + $4	underlay

Table 11. Palette and Overlay Select Truth Table (Two Plane Hardware Cursor Interfacing the Overlay Port) CR<11:10> = 10, B<16:13> = $F.

Circuit Description (continued)

Boundary Scan Testability Structures

As the complexity of RAMDACs increases, the need to easily access the RAMDAC for functional verification is becoming vital. The Bt463 has incorporated special circuitry that allows it to be accessed in full compliance with standards set by the Joint Test Action Group (JTAG). Conforming to the IEEE P1149.1 "Standard Test Access Port and Boundary Scan Architecture," Bt463 has dedicated pins which are used for testability purposes only.

JTAG's approach to testability utilizes boundary scan cells placed at each digital pin, both inputs and outputs. All scan cells are interconnected into a boundary-scan register (BSR) which applies or captures test data used for functional verification of the RAMDAC. JTAG is particularly useful for board testers using functional testing methods.

JTAG consists of four dedicated pins comprising the Test Access Port (TAP). These pins are TMS (Test Mode Select), TCK (Test Clock), TDI (Test Data Input), and TDO (Test Data Out). Complete verification of the RAMDAC can be achieved through these four TAP pins. With boundary-scan cells at each digital pin, the Bt463 has the capability to apply and capture the logic level. Since all of the digital pins are interconnected as a long shift register, the TAP logic has access and control of all the necessary pins to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry. The output result is scanned out on the TDO pin and externally checked. While isolating the Bt463 from the other components on the board, the user has easy access to all Bt463 digital pins through the TAP and can perform complete functionality tests without using expensive bed-of-nails testers.

The bidirectional MPU port is given special attention with respect to JTAG. Because JTAG requires control over each digital pin, an additional output enable (OE) function is included in the BSR for the MPU pins. In conjunction with the JTAG instruction, the output enable will configure the MPU port as an input or output.

With the JTAG bus, users also have access to a vital portion of the Bt463, the Output Signature Analysis Register (See Figure 10). With access to this register, users can easily verify expected video data serially through the JTAG port. The OSAR is located between the lookup table and the inputs to the DACs.

The power-on reset (POR) circuitry ensures that the Bt463 initializes each pin to operate in a RAMDAC mode instead of a JTAG test mode during power-up sequence.

A variety of verification procedures can be performed through the TAP Controller. Through a set of eight instructions, the Bt463 can verify board connectivity at all digital pins, generate artificial pixel vectors on-chip, check signatures on system pixel streams, and scan vectors in and out of the pixel shifter and signature analysis register. The instructions are accessible through the use of a simple state machine. For full explanation and details of the Bt463 JTAG instruction set, please consult the Application Note Bt463 JTAG Implementation, available in 1991.

Circuit Description (continued)

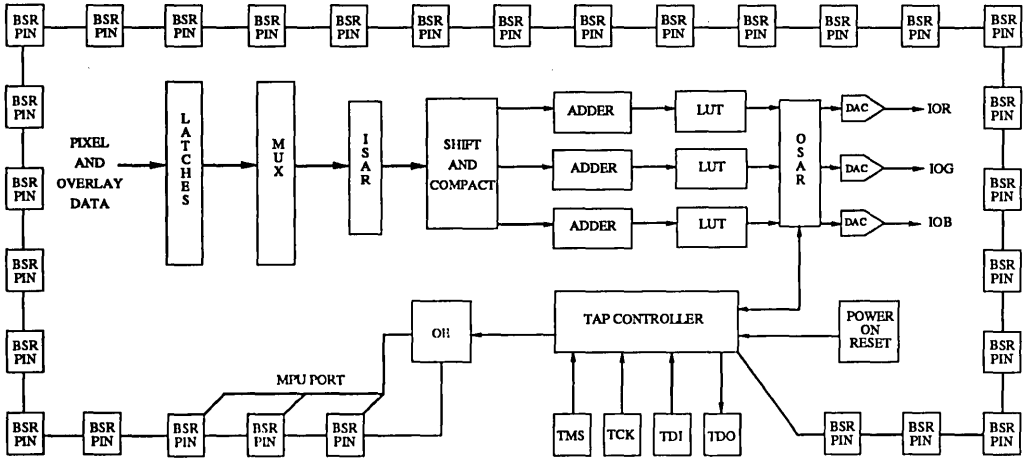


Figure 10. JTAG Block Diagram.

Internal Registers

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to data bus bit D0.

CR07, CR06 — Multiplex select

(00) reserved
(01) 4:1 multiplexing
(10) 1:1 multiplexing
(11) 2:1 multiplexing

These bits specify whether 1:1, 2:1, or 4:1 multiplexing is to be used for the pixel and overlay inputs. If 2:1 is specified, the {C} and {D} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be 1/2 the CLOCK rate. If 4:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be 1/4 the CLOCK rate. If 1:1 is specified, the {B}, {C}, and {D} inputs are ignored.

Note that in the 1:1 multiplex mode, the maximum clock rate is 66 MHz. LD* is used for the pixel clock. Although CLOCK is ignored in the 1:1 mode, it must remain running.

Note that it is possible to reset the pipeline delay of the Bt463 to a fixed 13 clock cycles. In this instance, each time the input multiplexing is changed, the Bt463 must again be reset to a fixed pipeline delay.

CR05, CR04 — reserved (logical zero)

CR03, CR02 — Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These two bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off). The counters that determine the blink rate are reset when command register_0 is written to.

CR01, CR00 — reserved (logical zero)

Internal Registers (continued)

Command Register_1

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR17 reserved (logical zero)

CR16 Overlay mapping

(0) Mapped to start address
(1) Mapped to common palette

Determines the physical address location of the overlay. In the standard mode, overlays are addressed with respect to the start address specified in the start address field of the window type table. The alternate mapping option addresses the same portion of the color map for overlays regardless of the start address location. For this mode, the overlays must be located at physical address locations $0201 - $020F.

CR15 Contiguous Plane Configuration

(0) 24/28 planes contiguous
(1) 12/16 planes contiguous

Allows the Bt463 to be used with 12- or 16-plane systems with an easy field upgrade to 24/28 planes. In the 12/16 plane configuration, up to 12 planes of true color are available. Red must be entered at P<3:0>, blue at P<4:7>, and green at P<11:8>. No shift is of use with 12-plane true color and the shift value in the window type word should be set to zero. The standard pseudo color mode is available, up to nine planes. In this mode, the shift value should be between 0 and either 11 (12-plane systems) or 15 (16 plane systems). In 16-plane systems, the 4 planes of overlay should be entered at P<15:12>. If the alternate location overlay is selected, then overlays are input at P<5,0,8,4> for the true color mode or at P<P+3:P> for the pseudo color mode. Unused pixel pins must be grounded.

CR14 Overlay planes select

(0) 4 overlay planes
(1) 8 overlay planes

Special mode which configures the Bt463 for 8 overlay planes. This mode can be used for either the standard true color or pseudo color display modes. For true color applications, the red pixel port corresponds to P0–P7, green corresponds P8–P15, and blue corresponds to P16–P23. The four least significant overlay bits, OL0–OL3 are assigned pixel port P24–P27. The window type port is converted into the four most significant bits of the overlay port where WT0–WT3 correspond to OL4–OL7, respectively. All 16 window type entries must be loaded and must be set to the same value. The recommended configuration is true color, no shift, 8 planes, all overlay inputs enabled, and the standard overlay location. Although different window display modes are no longer available, pixel operation is still user-defined based on the window type word placed in all 16 type entries. The only field with a restriction is the start address, which should have a value of 010000 ($0100). Thus, the physical location of the pixel lookup table and the overlay palette are preassigned, with the pixel color palette starting from $0100 and ending at $01FF while the overlay palette RAM is located at $0000 to $00FF.

Internal Registers (continued)

Command Register_1 (continued)

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR13	Window type entries (0) 16 entries (1) 14 entries	Determines the number of entries available in the window type table. If 14 entries are selected, then the two window type codes, $E and $F, correspond to cursor color 0 and cursor color 1 respectively.
CR12	Underlay enable (0) underlays disabled (1) underlays enabled	Determines the underlay availability. Once this bit is set to a logic one, underlays operation is achieved when the OL3 plane is a logic zero.
CR11–CR10	Overlay configuration (00) no cursor (01) one cursor plane (10) two cursor planes (11) reserved	Configures the overlay port so that overlay pins may be used as a hardware cursor port. By configuring this register, these overlay ports will directly address the cursor palette. If the overlay ports are used for cursors, they must be used on OL0 and OL1. OL0 is the least significant cursor bit. OL0 must be used for the single cursor mode. This overlay configuration register applies to the standard 4-plane mode or the eight-plane overlay option.

Internal Registers (continued)

Command Register_2

This register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to data bus bit D0.

CR27	Sync enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto IOG (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.
CR25–CR23	reserved (logical zero)	
CR22	Input SAR capture selection (0) lower 16 bits (1) upper 16 bits	This bit specifies whether the 16-bit input signature analysis register (SAR) should capture the lower or upper 16 bits of the pixel path.
CR21	Analysis register clock control (0) every LD* cycle (1) every CLOCK cycle	This bit controls the rate of operation of all signature analysis register (SAR) clocking. Logical zero is the normal mode, with pixel position (A, B, C, or D) determined by the test register. Logical one is a special mode for chip testing (in this instance, SAR operation is not guaranteed for clock rates above 30 MHz).
CR20	Test mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The signature analysis registers are used to hold the test result for both test methods.

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt463, the value read by the MPU will be $2A. Data written to this register is ignored.

Pixel Read Mask Register

The 28-bit pixel read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. The masking function is independent of all the operations specified by the window type entries, masking the pixel ports prior to pixel manipulation. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0, P8, P16, and P24.

Pixel Blink Mask Register

The 28-bit pixel blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. The blinking function is independent of all the operations specified by the window type entries, blinking the pixel ports prior to pixel manipulation. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0, P8, P16, and P24.

Revision Register

This 8-bit register is a read-only register, specifying the revision of the Bt463. The four most significant bits signify the revision letter in hexadecimal form. The four least significant bits do not represent any value and should be ignored.

Internal Registers (continued)

Red, Green, and Blue Output Signature Registers (OSAR)

Signature Operation

These three 8-bit signature registers may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the output signature registers while BLANK* is a logical zero to load the seed value. The output signature registers use data being loaded into the output DACs to calculate the signatures. JTAG logic can access the output signature analysis register independently of the MPU operation. MPU accesses to the output signature analysis registers require one address register load to address $020F followed by 3 reads or writes to the red, green, and blue signature registers, respectively. D0 corresponds to R0, G0, and B0.

When a test display is loaded into the frame buffer, a given value for the red, green, and blue signature registers will be returned if all circuitry is working properly.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the signature registers changes slightly. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A–D) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–D) is to be captured.

Input Signature Registers (ISAR)

Signature Operation

This 16-bit signature register may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the input signature register while BLANK* is a logical zero to load the seed value. The input signature register uses P0–P15 or P16–P27 and WT0–WT3 (selected by command bit CR22) to calculate the signatures. The 16 bits of data latched in the input signature register may be masked (forced low) by the read mask registers. MPU accesses to the input signature analysis register require one Address register load to $020E followed by 3 reads or writes to, respectively, lower byte, upper byte, and dummy access. D0 corresponds to P0 and P8 or to P16 and P24.

When a test display is loaded into the frame buffer, a given value for the input signature register will be returned if all circuitry is working properly.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the input signature register changes slightly. Rather than determining the signature, it just captures and holds the 16 bits of pixel data addressing the color palette RAM.

Each LD* cycle, the input signature register captures the 16 bits of pixel data addressing the color palette RAM. As only one of the (A–D) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–D) is to be captured.

Internal Registers (continued)

Test Register

This 8-bit register is used for testing the Bt463. If 1:1 pixel multiplexing is specified, signature analysis is done on every pixel; if 2:1 pixel multiplexing is specified, signature analysis is done on every second pixel; if 4:1 pixel multiplexing is specified, signature analysis is done on every fourth pixel. D0–D2 are used for 2:1 and 4:1 multiplexing to specify whether to use the A, B, C, or D pixel inputs, as follows:

D2 - D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	reserved
101	reserved
110	reserved
111	reserved

In 1:1 multiplexing mode, D0–D2 should select pixel A.

D3–D7 are used to compare the analog RGB outputs to each other and to a 145 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs or not, and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result

D7–D4		If D3 = 1	If D3 = 0
0000	normal operation	-	-
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 145 mV reference	red > 145 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 145 mV reference	green > 145 mV	green < 145 mV

The table above lists the valid comparison combinations. A logical one enables that function to be compared; the result is D3. The output levels of the DACs should be constant for 5 µs to allow enough time for detection. The capture occurs over one LD* period set by a logic one at any of the pixel pins P16A, P16B, P16C, or P16D.

For normal operation, D4–D7 must be a logical zero.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL-compatible). A logical zero drives the analog output to the blanking level, as illustrated in Tables 6 and 7. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL-compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 9 and 10). SYNC* does not override any other control or data input, as shown in Tables 6 and 7; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL-compatible). The P0–P27 {A–D}, WT0–WT3 {A–D}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is the output clock (1:1 multiplex mode) or is 1/2 or 1/4 of CLOCK, may be phase-independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the A.C. Characteristics section.
P0–P27 {A–D}	Pixel select inputs (TTL-compatible). These inputs are used to specify, on a pixel basis, which location of the color palette RAM is to be used to provide color information. The function of each of these pixel ports is configurable depending on the entry of the window type table. In fact, overlay data may exist from various locations of this pixel port. If data exists in the assigned overlay input port, then pixel data inputs are ignored. Overlay information (up to four bits per pixel) for either one, two, or four consecutive pixels are input through this port. Either one, two, or four consecutive pixels (up to 24 bits per pixel) are input through this port. All 4 pixels (112 bits) are latched on the rising edge of LD*. Unused inputs should be connected to GND. Note that typically the {A} pixel is output first, followed by the {B} pixel, etc., until all one, two, or four pixels have been output, at which point the cycle repeats.
WT0–WT3 {A–D}	Window type inputs (TTL-compatible). These inputs are latched on the rising edge of LD*. The window type references a location within the window type table which configures the corresponding pixel data or overlay data into user-defined display modes. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 13). All outputs, whether used or not, should have the same output load.
TCK	Test Clock (TTL-compatible). Used to synchronize all JTAG test structures. Maximum clock rate for this pin is 50 MHz. When not performing JTAG operations, this pin should be driven to a logic high.
TMS	Test Mode Select (TTL-compatible). JTAG input pin whose transitions drive the JTAG state machine through its sequences. When not performing JTAG operations, this pin should be driven to a logic high.
TDI	Test Data Input (TTL-compatible). JTAG input pin used for loading instructions to the TAP controller or for loading test vector data for boundary scan operation. When not performing JTAG operations, this pin should be driven to a logic high.
TDO	Test Data Output (TTL-compatible). JTAG output used for verifying test results of all JTAG sampling operations. This output pin is active for certain JTAG sequences, and will be 3-stated at all other times. When not performing JTAG operations, this pin should be left floating.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 11). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to *PC Board Layout Considerations* for critical layout criteria.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal (Figure 11). Note that the IRE relationships in Figures 9 and 10 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG is: RSET (ohms) = K1 * VREF (V) / IOG (mA) The full scale output current on IOR and IOB for a given RSET is: IOR, IOB (mA) = K2 * VREF (V) / RSET (ohms) where K1 and K2 are defined as:

Setup	IOG	IOR, IOB
7.5 IRE	K1 = 11,294	K2 = 8,067
0 IRE	K1 = 10,684	K2 = 7,457

VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 11, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 11. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL-compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Care should be taken to avoid glitches on this edge-triggered input.
R/W	Read/write control input (TTL-compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	Command control inputs (TTL-compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL-compatible). Data is transferred into and out of the device over this eight-bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions (continued)—169-pin PGA Package

Signal	Pin Number
BLANK*	J1
SYNC*	H1
LD*	H3
CLOCK*	J3
CLOCK	J2
P0A	F2
P0B	G3
P0C	F1
P0D	G1
P1A	F3
P1B	D1
P1C	E2
P1D	E1
P2A	C2
P2B	B1
P2C	D2
P2D	C1
P3A	C3
P3B	D3
P3C	E3
P3D	B2
P4A	A1
P4B	B3
P4C	C4
P4D	D4
P5A	A3
P5B	C5
P5C	A2
P5D	B4
P6A	A5
P6B	B6
P6C	A4
P6D	B5
P7A	A7
P7B	C7
P7C	A6
P7D	C6
P8A	A9
P8B	B8
P8C	A8
P8D	B7

Signal	Pin Number
P9A	A10
P9B	B10
P9C	B9
P9D	C10
P10A	A12
P10B	C11
P10C	A11
P10D	B11
P11A	A14
P11B	B12
P11C	A13
P11D	C12
P12A	A16
P12B	C13
P12C	A15
P12D	B13
P13A	C14
P13B	B15
P13C	A17
P13D	B14
P14A	D15
P14B	B16
P14C	E15
P14D	C15
P15A	D16
P15B	C17
P15C	C16
P15D	B17
P16A	T16
P16B	T17
P16C	R16
P16D	R17
P17A	R15
P17B	R14
P17C	P15
P17D	U17
P18A	T14
P18B	U15
P18C	T15
P18D	U16

Signal	Pin Number
P19A	T13
P19B	U13
P19C	R13
P19D	U14
P20A	R12
P20B	U11
P20C	T12
P20D	U12
P21A	T11
P21B	U9
P21C	R11
P21D	U10
P22A	R10
P22B	U8
P22C	T10
P22D	T9
P23A	T7
P23B	U6
P23C	T8
P23D	U7
P24A	R6
P24B	U4
P24C	R7
P24D	U5
P25A	T5
P25B	U2
P25C	T6
P25D	U3
P26A	T4
P26B	R4
P26C	R5
P26D	U1
P27A	R3
P27B	N3
P27C	T3
P27D	T1
TMS	D17
TCK	E16
TDI	E17
TDO	F17

Pin Descriptions (continued)—169-pin PGA Package

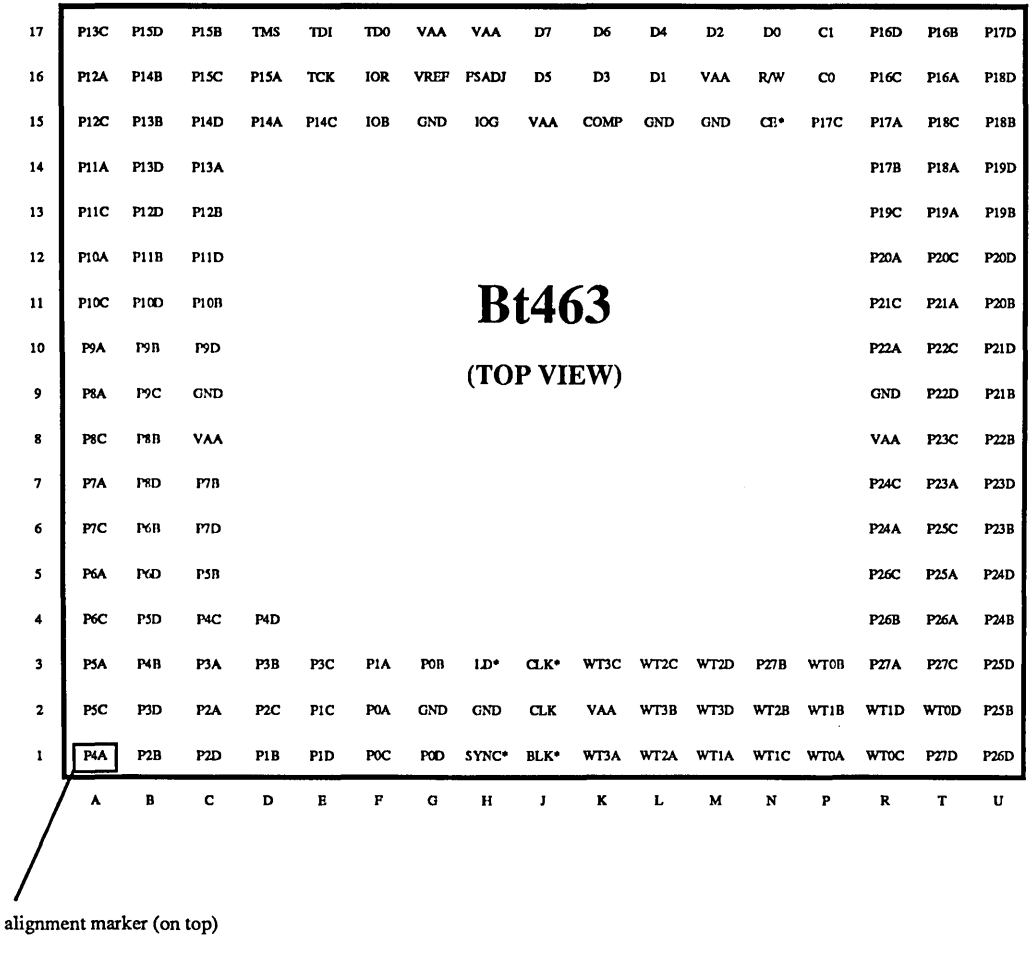
Signal	Pin Number
WT0A	P1
WT0B	P3
WT0C	R1
WT0D	T2
WT1A	M1
WT1B	P2
WT1C	N1
WT1D	R2
WT2A	L1
WT2B	N2
WT2C	L3
WT2D	M3
WT3A	K1
WT3B	L2
WT3C	K3
WT3D	M2
D0	N17
D1	L16
D2	M17
D3	K16
D4	L17
D5	J16
D6	K17
D7	J17

Signal	Pin Number
IOR	F16
IOG	H15
IOB	F15
COMP	K15
FS ADJUST	H16
VREF	G16
CE*	N15
R/W	N16
C1	P17
C0	P16

Signal	Pin Number
VAA	C8
VAA	G17
VAA	H17
VAA	J15
VAA	K2
VAA	R8
VAA	M16
GND	C9
GND	G2
GND	G15
GND	H2
GND	L15
GND	M15
GND	R9

4

Pin Descriptions (continued)—169-pin PGA Package



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
17	P13C	P15D	P15B	TMS	TDI	TD0	VAA	VAA	D7	D6	D4	D2	D0	C1	P16D	P16B	P17D
16	P12A	P14B	P15C	P15A	TCK	IOR	VREF	PSADJ	D5	D3	D1	VAA	R/W	C0	P16C	P16A	P18D
15	P12C	P13B	P14D	P14A	P14C	IOB	GND	IOG	VAA	COMP	GND	GND	CE*	P17C	P17A	P18C	P18B
14	P11A	P13D	P13A												P17B	P18A	P19D
13	P11C	P12D	P12B												P19C	P19A	P19B
12	P10A	P11B	P11D												P20A	P20C	P20D
11	P10C	P10D	P10B												P21C	P21A	P20B
10	P9A	P9B	P9D												P22A	P22C	P21D
9	P8A	P9C	GND												GND	P22D	P21B
8	P8C	P8B	VAA												VAA	P23C	P22B
7	P7A	P8D	P7B												P24C	P23A	P23D
6	P7C	P6B	P7D												P24A	P25C	P23B
5	P6A	P6D	P5B												P26C	P25A	P24D
4	P6C	P5D	P4C	P4D											P26B	P26A	P24B
3	P5A	P4B	P3A	P3B	P3C	P1A	P0B	LD*	CLK*	WT3C	WT2C	WT2D	P27B	WT0B	P27A	P27C	P25D
2	P5C	P3D	P2A	P2C	P1C	P0A	GND	GND	CLK	VAA	WT3B	WT3D	WT2B	WT1B	WT1D	WT0D	P25B
1	P4A	P2B	P2D	P1B	P1D	P0C	P0D	SYNC*	BLK*	WT3A	WT2A	WT1A	WT1C	WT0A	WT0C	P27D	P26D

Pin Descriptions (continued)—169-pin PGA Package

	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
17	P17D	P16B	P16D	C1	D0	D2	D4	D6	D7	VAA	VAA	TD0	TDI	TMS	P15B	P15D	P13C
16	P18D	P16A	P16C	C0	R/W	VAA	D1	D3	D5	FSADJ	VREF	IOR	TCK	P15A	P15C	P14B	P12A
15	P18B	P18C	P17A	P17C	CE*	GND	GND	COMP	VAA	IOG	GND	IOB	P14C	P14A	P14D	P13B	P12C
14	P19D	P18A	P17B												P13A	P13D	P11A
13	P19B	P19A	P19C												P12B	P12D	P11C
12	P20D	P20C	P20A												P11D	P11B	P10A
11	P20B	P21A	P21C												P10B	P10D	P10C
10	P21D	P22C	P22A					(BOTTOM VIEW)							P9D	P9B	P9A
9	P21B	P22D	GND												GND	P9C	P8A
8	P22B	P23C	VAA												VAA	P8B	P8C
7	P23D	P23A	P24C												P7B	P8D	P7A
6	P23B	P25C	P24A												P7D	P6B	P7C
5	P24D	P25A	P26C												P5B	P6D	P6A
4	P24B	P26A	P26B											P4D	P4C	P5D	P6C
3	P25D	P27C	P27A	WT0B	P27B	WT2D	WT2C	WT3C	CLK*	LD*	P0B	P1A	P3C	P3B	P3A	P4B	P5A
2	P25B	WT0D	WT1D	WT1B	WT2B	WT3D	WT3B	VAA	CLK	GND	GND	P0A	P1C	P2C	P2A	P3D	P5C
1	P26D	P27D	WT0C	WT0A	WT1C	WT1A	WT2A	WT3A	BLK*	SYNC*	P0D	P0C	P1D	P1B	P2D	P2B	P4A

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in *Bt451/7/8 Evaluation Module Operation and Measurements*, application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt463 power and ground lines by shielding the digital inputs and providing good decoupling. Trace lengths between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a six-layer PC board is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferably analog ground plane), layer 3 the analog power plane, with the remaining layers used for digital traces and digital power supplies.

The optimum layout enables the Bt463 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8 inch gap) connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inch from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground partitioning isolation technique is constrained by the noise margin constraint during digital readback of the Bt463.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk. For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and VREF circuitry should be used, as shown in Figure 11. Another isolated ground plane should be used for the GND pins of the Bt463 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt463 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8 inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 11, located within three inches of the Bt463. This bead provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged such that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each of four groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 33 µF capacitor is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low frequency supply noise will require a larger value. Lead lengths should be minimized for best performance so that the self-resonance frequency is greater than the LD* frequency.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt463 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot, which can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. Prevention is done by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt463 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a load resistor and a termination resistor equal to the transmission line impedance. The load resistor connection between the current output and GND should be as close as possible to the Bt463 to minimize reflections. Unused analog outputs should be connected to GND.

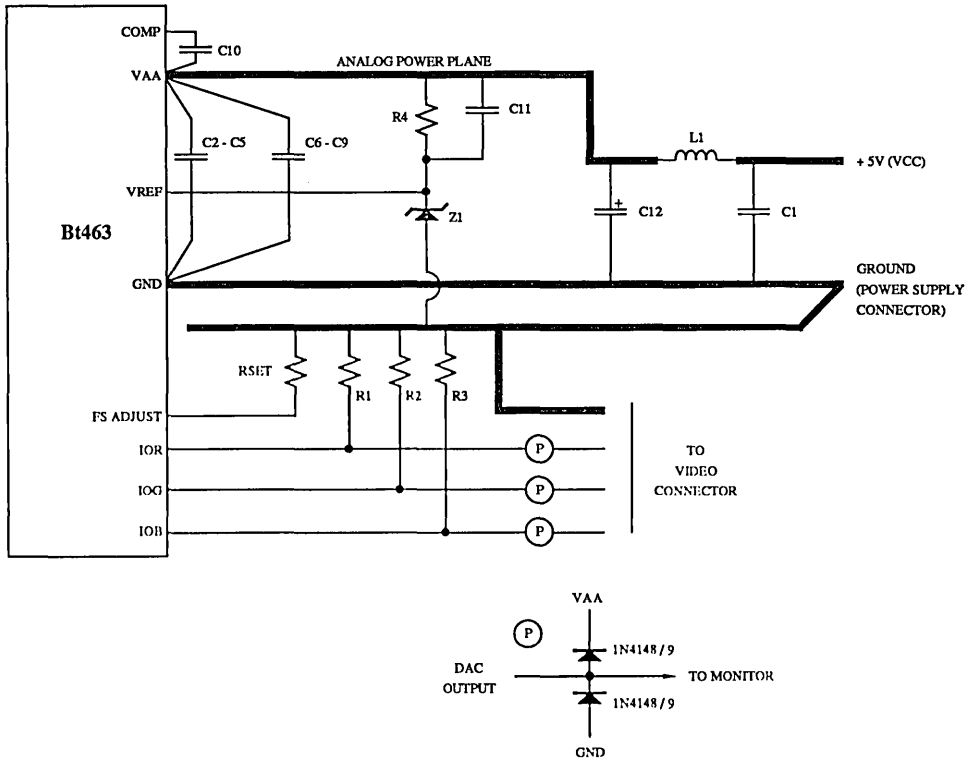
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, helping to alleviate EMI and noise problems.

Analog Output Protection

The Bt463 analog outputs should be protected against high energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 11 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. This protection circuit should be located as close to the driver as possible. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt463.

Figure 11. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Due to the high clock rates at which the Bt463 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (typically a 220-ohm resistor to VCC and a 330-ohm resistor to GND). The termination resistors should be as close as possible to the Bt463.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt463 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by two or four (depending on whether 2:1 or 4:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase-shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

For display applications where a single Bt463 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 input multiplexing of the Bt463, and will also optionally set the pipeline delay of the Bt463 to 13 clock cycles. The Bt438 may also be used to interface the Bt463 to a TTL clock. Figure 12 illustrates using the Bt438 with the Bt463.

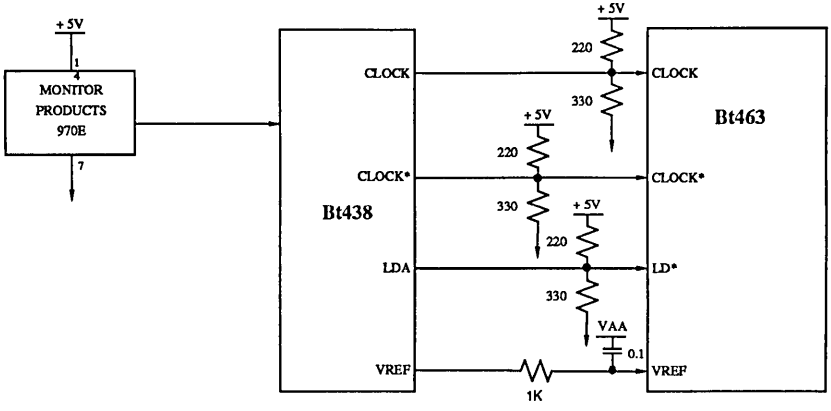


Figure 12. Generating the Bt463 Clock Signals.

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt463, although fixed after a power-up condition, may be anywhere from 11 to 15 clock cycles. The Bt463 contains additional circuitry enabling the pipeline delay to be fixed at 13 clock cycles. The Bt438 Clock Generator Chip supports this mode of operation when used with the Bt463.

To reset the Bt463, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for **at least** three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

Resetting the Bt463 to a 13 clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if multiple Bt463s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

ESD and Latchup Considerations

ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Application Information (continued)

Test Features of the Bt463

The Bt463 contains two dedicated test registers and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section is intended to explain the operating usage of these test features.

Signature Registers (Signature Mode)

The input signature register is 16 bits wide, capturing pixel information prior to the lookup tables. Since the pixel path is 28 bits wide, the lower or upper 16 bits are selected for capture via command bit CR22.

The output signature register, in the active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color, and are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as the three on-chip DACs.

The SARs act as a 16-bit or 24-bit wide Linear Feedback Shift Register on each succeeding pixel that is latched. It is important to note that in either the 2:1 or 4:1 multiplexed modes the SARs only latch one pixel per "load group." Thus, the SARs are operating on only every second or fourth pixel in the multiplexed modes. The user determines which pixel phase (A, B, C, or D) is latched for generating new signatures by setting bits D0–D2 in the Test Register.

In 1:1 mux mode, the SARs will generate signatures on each succeeding pixel in the input stream. In this case, the user should always select pixel "A" (Test Register D0, D1, and D2 = 000) when in the 1:1 mode, since the "A" pixel pins are the only active pixel inputs.

The Bt463 will only generate signatures while in "active-display" (BLANK* negated). The SARs are available for reading and writing via the MPU port when the Bt463 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 16-bit or 24-bit "seed" value into the SARs. Then, a known pixel stream will be input to the chip, say one scan-line or one frame buffer worth of pixels. Then, at the succeeding blank state, the resultant 16-bit or 24-bit signature canbe read out by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay and cursor data validity is also tested using the signature registers.

Assuming the chip is running 2:1 or 4:1 mux modes, the above process would be repeated with all different pixel phases—A, B, C, or D—being selected.

It is not simple to describe algorithmically the specific linear feedback shift operation used in the Bt463. The linear feedback configurations are shown in Figures 13 and 14.

Experienced users have developed tables of specific seeds and pixel streams and recorded the signatures that result from those inputs applied to "known-good" parts. Note that a good signature from one given pixel stream can by used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed and the succeeding pixel stream fed to the SARs.

Signature Registers (Data Strobe Mode)

Setting command bit CR20 to a logic one puts the SARs into data strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the SARs from generating signatures. Instead, the SARs simply capture and hold the respective pixel phase selected.

Any MPU data written to the SARs is ignored. One use, however, is to directly check each pixel color value that is strobed into the SARs. To read out values captured in the middle of a pixel stream, the user should first freeze all inputs to the Bt463. The levels of most inputs do not matter EXCEPT that CLOCK should be high, and CLOCK* should be low. Then, the user may read out the pixel color by doing three successive MPU reads from the red, green, and blue SARs, respectively. Likewise, the input SAR may be read with 2 MPU reads.

In general, the color read-out will correspond to a pixel latched on the previous load. However, due to the pipelined data path, the color may come from an earlier load cycle. To read successive pixels, toggle LD*, pulse the CLOCK pins according to the mux state (1, 2, or 4 periods), then hold all pixel-related inputs and perform the three MPU reads as described. This process is best done on a sophisticated VLSI semiconductor tester.

Application Information (continued)

Analog Comparator

The other dedicated test structure in the Bt463 is the analog comparator. It allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected via the Test Register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the Test Register. The capture occurs over one LD* period set by a logic one at pixel port P16 (A–D).

Due to the simple design of the comparator, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, up until capture.

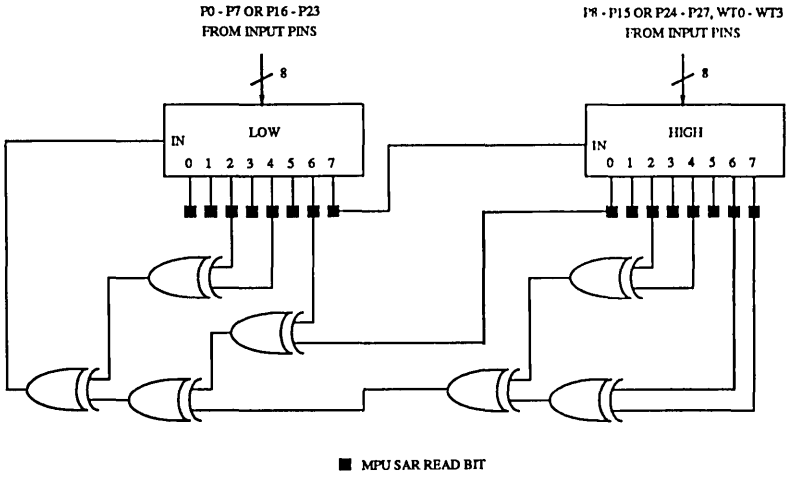


Figure 13. Input Signature Analysis Register Circuit.

Application Information (continued)

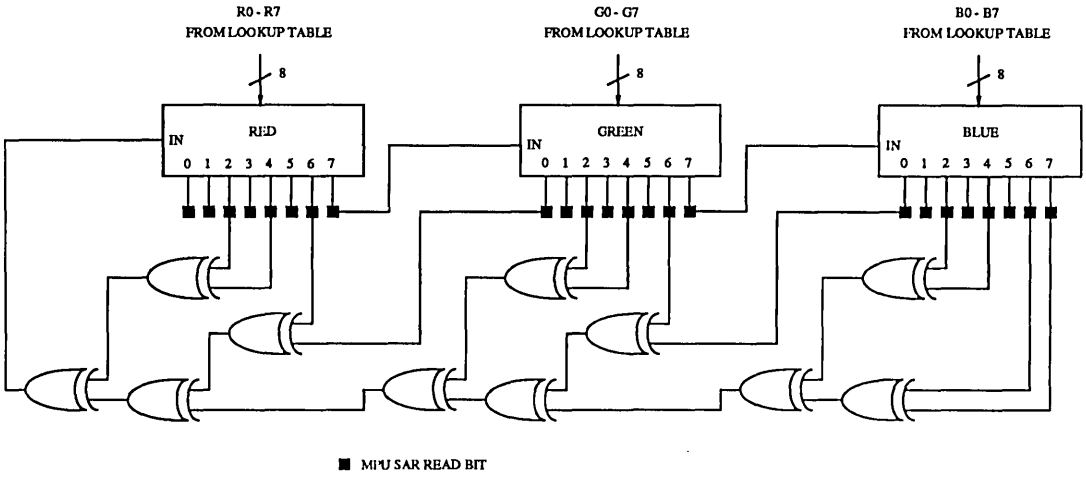


Figure 14. Output Signature Analysis Register Circuit.

Application Information (continued)

Initializing the Bt463

Following a power-on sequence, the Bt463 must be initialized. This sequence will configure the Bt463 as follows:

4:1 multiplexed operation
4 overlay planes on P<27:23>
sync enabled on IOG, 7.5 IRE blanking pedestal
no cursor interface
24-plane true color
start address at $0001
16 window entries

Control Register Initialization

	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register 0	10
Write $00 to command register 1	10
Write $C0 to command register 2	10
Write $00 to reserved location	10
Write $FF to pixel read mask register P0- P7	10
Write $FF to pixel read mask register P8- P15	10
Write $FF to pixel read mask register P16- P23	10
Write $FF to pixel read mask register P24- P27	10
Write $00 to pixel blink mask register P0- P7	10
Write $00 to pixel blink mask register P8-P15	10
Write $00 to pixel blink mask register P16- P23	10
Write $00 to pixel blink mask register P24- P27	10
Write $00 to test register	10
Write $00 to address register low	00
Write $03 to address register high	01
Write $00 to B0-B7 register (location $0)	10
Write $E1 to B8-B15 register (location $0)	10
Write $03 to B16-B23 register (location $0)	10
Write $00 to B0-B7 register (location $1)	10
Write $E1 to B8-B15 register (location $1)	10
Write $03 to B16-B23 register (location $1)	10
:	:
Write $00 to B0-B7 register (location $F)	10
Write $E1 to B8-B15 register (location $F)	10
Write $03 to B16-B23 register (location $F)	10

Color Palette RAM Initialization

Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $000)	11
Write green data to RAM (location $000)	11
Write blue data to RAM (location $000)	11
Write red data to RAM (location $001)	11
Write green data to RAM (location $001)	11
Write blue data to RAM (location $001)	11
:	:
Write red data to RAM (location $20F)	11
Write green data to RAM (location $20F)	11
Write blue data to RAM (location $20F)	11

Cursor Color Palette Initialization

Write $00 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2)*	10
Write green data to cursor (location $2)*	10
Write blue data to cursor (location $2)*	10
Write red data to cursor (location $3)*	10
Write green data to cursor (location $3)*	10
Write blue data to cursor (location $3)*	10

* Even though cursor locations $2 and $3 are not accessible, they must still be initialized in order for the cursor palette to operate correctly.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.20	1.235	1.26	Volts
FS ADJUST Resistor	RSET		523		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	Volts
Voltage on Any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
PGA	TJ			+170	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
(except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			60	µA
Input Low Current (Vin = 0.4 V)	IIL			-60	µA
Input Capacitance	CIN		4	10	pF
(f = 1 MHz, Vin = 2.4 V)					
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	.6		6	Volts
Input High Current (Vin = 4.0V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			-1	µA
Input Capacitance	CKIN		4	10	pF
(f = 1 MHz, Vin = 4.0V)					
Digital Outputs (D0-D7)					
Output High Voltage	VOH	2.4			Volts
(IOH = 400 µA)					
Output Low Voltage	VOL			0.4	Volts
(IOL = 3.2 mA)					
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Blank Level on IOR, IOB		0	5	50	µA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.2	Volts
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		90		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

A C Characteristics

Parameter	Symbol	Min/Typ/ Max	170 MHz	135 MHz	110 MHz	Units
Clock Rate	Fmax	max	170	135	110	MHz
LD* Rate	LDmax					
1:1 multiplexing		max	67.5	67.5	55	MHz
2:1 multiplexing		max	67.5	67.5	55	MHz
4:1 multiplexing		max	42.5	33.75	27.5	MHz
R/W, C0, C1 Setup Time	1	min	0	0	0	ns
R/W, C0, C1 Hold Time	2	min	15	15	15	ns
CE* Low Time	3	min	50	50	50	ns
CE* High Time	4	min	25	25	25	ns
CE* Asserted to Data Bus Driven	5	min	7	7	7	ns
CE* Asserted to Data Valid	6	max	75	75	75	ns
CE* Negated to Data Bus 3-Stated	7	max	15	15	15	ns
Write Data Setup Time	8	min	35	35	35	ns
Write Data Hold Time	9	min	3	3	3	ns
TMS, TDI Setup Time	10	min	8	8	8	ns
TMS, TDI Hold Time	11	min	6	6	6	ns
TCK Low Time	12	min	10	10	10	ns
TCK High Time	13	min	10	10	10	ns
TCK Asserted to TDO Driven	14	min	5	5	5	ns
TCK Asserted to TDO Valid	15	max	12	12	12	ns
TCK Negated to TDO 3-Stated	16	max	12	12	12	ns
Pixel and Control Setup Time	17	min	3	3	3	ns
Pixel and Control Hold Time	18	min	2	2	2	ns
Clock Cycle Time	19	min	5.88	7.4	9.09	ns
Clock Pulse Width High Time	20	min	2.5	3.2	4	ns
Clock Pulse Width Low Time	21	min	2.5	3.2	4	ns
LD* Cycle Time	22					
1:1 multiplexing		min	14.81	14.81	18.18	ns
2:1 multiplexing		min	14.81	14.81	18.18	ns
4:1 multiplexing		min	23.53	29.63	36.36	ns
LD* Pulse Width High Time	23					
1:1 multiplexing		min	6	6	7	ns
2:1 multiplexing		min	5	6	8	ns
4:1 multiplexing		min	9	12	15	ns
LD* Pulse Width Low Time	24					
1:1 multiplexing		min	6	6	7	ns
2:1 multiplexing		min	5	6	8	ns
4:1 multiplexing		min	9	12	15	ns

See test conditions on next page.

AC Characteristics (continued)

Parameter	Symbol	Min/Typ/ Max	170 MHz	135 MHz	110 MHz	Units
Analog Output Delay	25	typ	12	12	12	ns
Analog Output Rise/Fall Time	26	typ	1.5	1.5	1.5	ns
Analog Output Settling Time	27	max	8	8	8	ns
Clock and Data Feedthrough*		typ	tbd	tbd	tbd	dB
Glitch Impulse*		typ	50	50	50	pV - sec
DAC to DAC Crosstalk		typ	tbd	tbd	tbd	dB
Analog Output Skew		typ	0	0	0	ns
		max	2	2	2	ns
Pipeline Delay		min	11	11	11	Clocks
		max	15	15	15	Clocks
VAA Supply Current**	IAA	typ	550	500	450	mA
		max	tbd	tbd	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. TTL input values are 0-3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA-0.8 to VAA-1.8 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 18. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C. IAA (max) at VAA = 5.25 V, TA = 0° C.

Timing Waveforms

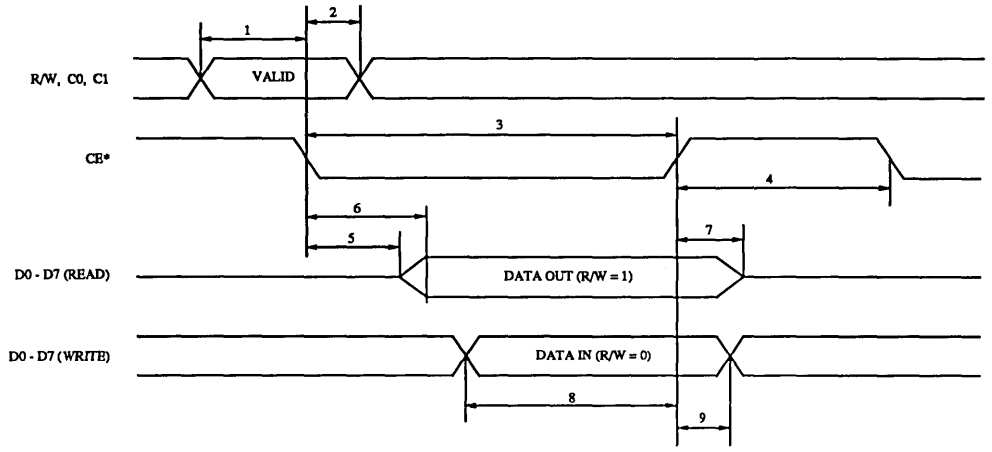
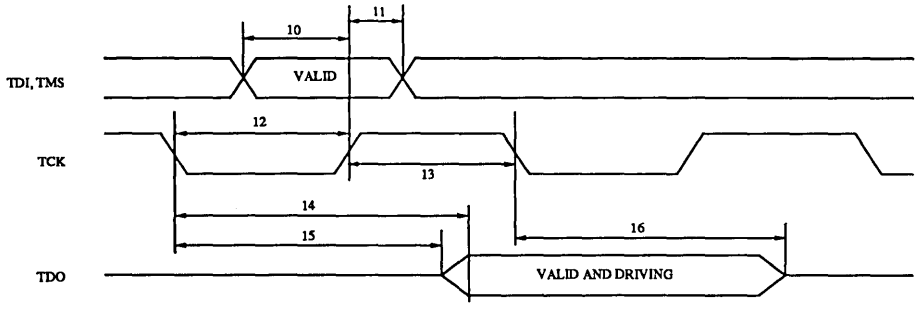


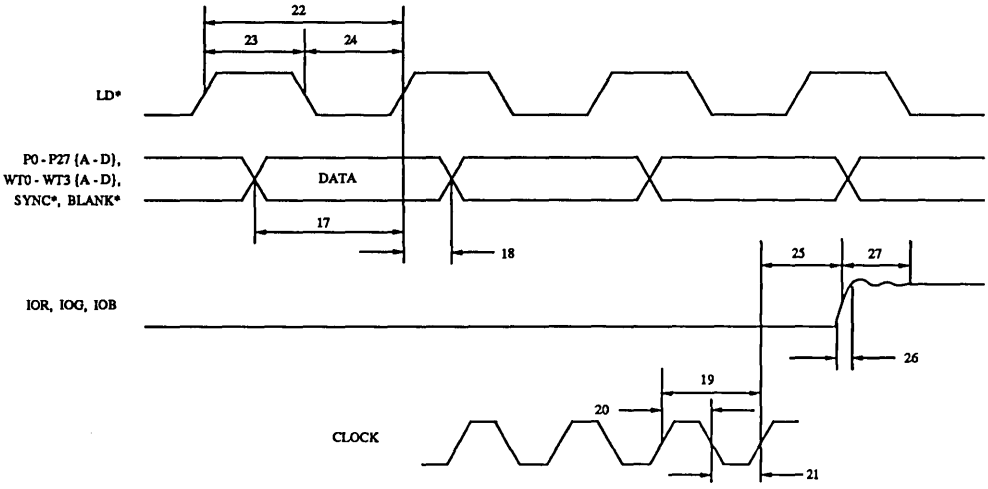
Figure 15. MPU Read/Write Timing Dimensions.



Note 1: TMS and TDI are sampled on the rising edge of TCK

Note 2: TDO changes after the falling edge of TCK

Figure 16. JTAG Timing.



Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full-scale transition.

Note 2: Output settling time measured from 50% point of full-scale transition to output settling within ±1LSB.

Note 3: Output rise/fall time measured between 10% and 90% points of full-scale transition.

Figure 17. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt463KG170	170 MHz	169-pin Ceramic PGA	0° to +70° C
Bt463KG135	135 MHz	169-pin Ceramic PGA	0° to +70° C
Bt463KG110	110 MHz	169-pin Ceramic PGA	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
B	Additional information on start address and true-color operation.